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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,001	11/08/2000	Matthew B. Haycock	884.302US1	3143

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EXAMINER

CHANG, ERIC

ART UNIT PAPER NUMBER

2116

DATE MAILED: 08/11/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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**Office Action Summary**

Application No.

09/709,001

Applicant(s)

HAYCOCK ET AL.

Examiner

Eric Chang

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 May 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 23-26 and 28-30 is/are allowed.  
6) ☒ Claim(s) 1-22 and 27 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

1. Claims 1-30 are pending.
2. Claims 23-26 and 28-30 are allowable.

***Response to Arguments***

3. Applicant's arguments with respect to claims 23-26 and 28-30 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
5. Claims 1-2, 4-10, 13-16, 20-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,268,932 to Okuzono.
6. As to claim 1, Okuzono discloses a digital bus comprising:
  - [a] a transmitter generating a plurality of clock signals [col. 10, lines 47-51];
  - [b] a receiver comprising one or more FIFO units [col. 11, lines 5-18]; and
  - [c] a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal [FIG. 1, elements 104-105 and 108, col. 6, lines 20-34, col. 10, lines 47-67, and col. 11, lines 1-26];

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[d] wherein each of the plurality of reset signals has a latency of less than or equal to a clock cycle with the reset signal [col. 12, lines 8-14]; and

[e] a transmission medium to couple the plurality of clock signals from the transmitter to the receiver [col. 10, lines 47-51].

Okuzono teaches a digital bus receiving a plurality of clock signals from a transmitter, and using a synchronizer to generate a plurality of reset signals to control the flow of data through a plurality of FIFO units based on the plurality of received clock signals and a master sample clock, in order to synchronize the data received over the bus, substantially as claimed. Furthermore, Okuzono teaches that the frame phases of the transmission frames are required to be aligned in the transmission line interface circuit [col. 1, lines 26-39]; it would be obvious to one of ordinary skill in the art that if the plurality of write reset signals had a latency of greater than one clock cycle, the write reset signals would no longer be synchronized with the read reset signal. Therefore, each of the plurality of reset signals has a latency of less than or equal to a clock cycle with the reset signal, substantially as claimed.

7. As to claim 2, Okuzono discloses the transmitter comprises a transceiver [FIG. 1, element 101].

8. As to claims 4-5, Okuzono discloses the phase of one of the plurality of clock signals may be behind the phase of another one of the plurality of clock signals [col. 2, lines 45-53]. It would have been obvious to one of ordinary skill in the art that the phase difference could

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comprise 180 degrees, or have a skew of less than 90 degrees, or any other difference in phase, substantially as claimed.

9. As to claim 6, Okuzono discloses the transmission medium transfers high bit rate data [col. 1, lines 50-53]. In addition, Self teaches that the communications rate would be upwards of 200 MHz [col. 2, lines 31-42], such as 500 MHz to 5 GHz, substantially as claimed.

10. As to claims 7, 9-10 and 16, Okuzono discloses a transmission line [col. 1, lines 50-53]. It is well known in the art that such a transmission line may comprise any well known means for communicating data from a transmitter to a receiver, such as a cable, metal interconnects, or free space, substantially as claimed.

11. As to claim 8, Okuzono discloses synchronizing the received clocks with master sample clock [col. 1, lines 59-66]. Okuzono further teaches a frequency dividing circuit that generates the reset signals relative to the received clocks [col. 6, lines 35-43], such as at twice the frequency of the received clocks, substantially as claimed.

12. As to claims 13-15, Okuzono discloses a digital bus comprising a transmitter generating a plurality of clock signals, a receiver comprising one or more FIFO units, and a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal to synchronize flow of data through the FIFO units, substantially as claimed. Because Okuzono teaches the digital bus, Okuzono teaches

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an integrated circuit comprising said elements. Furthermore, it is well known in the art that an integrated circuit may be fabricated on a single silicon substrate, substantially as claimed.

13. As to claims 20-22, Okuzono discloses a digital bus comprising a transmitter generating a plurality of clock signals, a receiver comprising one or more FIFO units, and a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal to synchronize flow of data through the FIFO units, substantially as claimed. Because Okuzono teaches the digital bus comprising such a synchronizer unit, Okuzono teaches the synchronizer unit. Furthermore, it is well known in the art that a logic circuit may comprise complementary metal-oxide semiconductor logic circuits, and that said circuits have a delay of less than about two nanoseconds, substantially as claimed.

14. As to claim 27, Okuzono discloses a method for synchronizing data from a FIFO using a reset signal based a plurality of clock signals, a master sample clock signal, and a reset signal [col. 6, lines 20-34, col. 10, lines 47-67, and col. 11, lines 1-48]. Okuzono teaches generating an intermediate clock as a synchronized reset signal to reset the plurality of latching means in order to synchronize the data, substantially as claimed.

15. Claims 3, 11-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,268,932 to Okuzono, in view of U.S. Patent 5,634,043 to Self et al.

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16. As to claims 3, 11-12 and 17-19, Okuzono discloses the transmitter comprises a transceiver that transfers high bit rate data [FIG. 1, element 101, and col. 1, lines 50-53], and the receiver comprises data terminal equipment that receives high bit rate data [FIG. 1, element 106, and col. 1, lines 50-53]. Okuzono teaches all of the limitations of the claim, but does not teach that the transmitter is a processor or that the receiver is a memory.

Self teaches that data is transferred between a transmitting processor and a receiving memory at a high bit rate [Abstract, and col. 1, lines 7-20]. Thus, Self teaches a high-speed data transfer synchronization similar to that of Okuzono. Self further teaches that the data is transferred between a processor and a memory, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the communications between a processor and a memory as taught by Self. One of ordinary skill in the art would have been motivated to do so that the data would be transferable to a memory for storage.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of synchronizing high bit rate data between a transmitter and a receiver. Moreover, the communications path means taught by Self would improve the utility of Okuzono because it allowed the teachings to be specifically be applied to processor/memory data, thereby allowing the data to be saved and retrieved at a high data rate. In addition, it would have been obvious to one of ordinary skill in the art that the receiver be any memory that receives high bit rate data, such as DRAM or SRAM memory, substantially as claimed.

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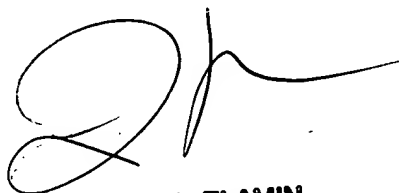
***Conclusion***

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ec  
August 2, 2004



**A. ELAMIN  
PRIMARY EXAMINER**